REMARKS

I.   Specification

The Examiner objected to the Abstract because it lacks narrative format and merely paraphrases claim 1.

Accordingly, the abstract has been amended in order to remove this objection.

II.   Claim Rejections Under 35 U.S.C. § 102

The Examiner rejected claims 1-15, 18 & 19 under 35 U.S.C. § 102(e) as being anticipated by Roesner et al, hereinafter "Roesner" (U.S. PG Pub 2004/0216077).

Regarding independent claims 1 and 8 the Examiner argued that Roesner discloses a method and system for automatically verifying a hardware design based on a hardware specification document (pg. 2 ¶28) comprising the steps of:

designating a plurality of predefined elements within a hardware specification document, wherein said hardware specification document (--configuration specification files and HDL files--) provides a hardware design for a hardware device (pg. 2, ¶26- ¶27, and fig. 8, elements 800,802, pg. 10-11, ¶137-139);

storing said plurality of predefined elements within a database of hardware components (--configuration database--), wherein each predefined element of said plurality of predefined elements is associated with a hardware component of said hardware device (fig. 8, element 814, and pg. 11, ¶140); and

automatically comparing (--verifying/detecting/matching--) physical components of said hardware device with said predefined elements maintained within said database of said hardware components (pg. 1, ¶21-22; ¶166; fig. 8, ¶143; fig. 15, ¶223-225; and pg. 25, ¶276- ¶277- verifying /comparing the function/ logic circuit level design and high-level design --) upon an initial power-up

(--initialization power-on or firmware system --) of said hardware device, in order to verify (--testing or debugging--) that said hardware device functions according to said hardware specification document (pg.23, ¶258-260 and pg. 25, ¶263-275).

The Applicant has amended claim 1 further to distinguish the claim from the cited prior art, in particular Roesner. Amended claim 1 reads as follows:

A method for automatically verifying a hardware design based on a hardware specification document, said method comprising the steps of:

designating a plurality of predefined elements within a hardware specification document, wherein said hardware specification document provides a hardware design for a hardware device;

storing said plurality of predefined elements within a database of hardware components, wherein each predefined element of said plurality of predefined elements is associated with a hardware component of said hardware device;

embedding said plurality of predefined elements within said hardware specification document preparatory to storing said predefined elements in said database, wherein said plurality of predefined elements comprise flags which can be utilized by a document reader script;

creating at least one RTL Hardware Description code file from said database, said RTL Hardware description code file(s) defining said predefined elements stored in said database; and

automatically comparing physical components of said hardware device with said predefined elements maintained within said database of said hardware components upon an initial power-up of said hardware device, in order to verify that said hardware device functions according to said hardware specification document.

The scope of claim 1 has been limited to the method step of creating at least one RTL Hardware Description code file from the database, the RTL Hardware description code file(s) defining the predefined elements stored in the database. Also, the claim has been limited to the method step of embedding the plurality of predefined elements within the specification hardware document preparatory to storing the plurality of predefined elements in the database and, predefined elements comprising flags which can be utilized by a document reader script.

Roesner discloses methods, systems and program products for specifying the configuration of a digital system described by a hardware description language (HDL) (pg. 2, ¶0028 and FIG. 1). Roesner does not disclose creating at least one RTL Hardware Description code file from a database. Unlike amended claim 1, Roesner discloses a method in which the specification document originates in HTL language making it extremely difficult for designers to view operational information during design of the circuit so that users of the method disclosed in Roesner would, in practice, have to maintain a separate specification document for the purpose of designing hardware. Furthermore, there is nothing suggested in Roesner or the other citations to provide the method of amended claim 1.

Creating at least one RTL Hardware Description code file from the database and comparing the physical components, as now claimed in claim 1, is advantageous in that the verification method creates HTL language from the database after designating and storing the predefined elements in the database. Users designing hardware, such as circuits, work from a specification document which is in a language other than HTL or other high level languages because operational information which the user requires to access is buried obscurely and deeply in a HTL document. Embedding the predefined elements in the specification document using flags preparatory to storing the predefined elements in the database, as now claimed in claim 1, permits the user to easily view and modify operational information during the design or development of the circuit and still change the document into RTL code for the purpose of testing the functionality of

the circuit. Consequently, a single specification document can be used for the purpose of the user designing the hardware and for the purpose of verifying the functionality of the hardware.

System claims 8 & 18 have been limited to an RTL auto-generation module for creating at least one RTL Hardware code from the database, and to reflect the fact that the plurality of predefined elements are embedded in the specification document preparatory to storing the elements in the database. As already mentioned in the preceding paragraph, Roesner discloses a system in which the specification document originates in HTL language and there is nothing disclosed or suggested in Roesner to provide an RTL auto-generation module as claimed in amended claims 8 or 18.

The Applicant notes that in order to succeed in a rejection to one or more claims under 35 U.S.C. § 102(e) based on a prior art reference, the prior art reference must disclose all of the limitations and features of the rejected claim or claims. If the prior art reference lacks even one feature/limitation of the rejected claim, the rejection must be withdrawn. In this case, the Roesner reference does not teach all of the limitations and features of the Applicant's amended claims 1 , 8 & 18.

Claims 2-7, 9-15 and 19 were rejected in part as dependent on claims 1, 8 and 18. Traversing the rejections of claims 1, 8 and 18 leads to traversing the rejections of claims 2-7, 9-15 and 19.

Notwithstanding the foregoing, claims 3-5 and 11-13 have been amended to provide adequate protection to important novel features in view of the cited prior art. In particular, claim 3 has been amended to recite that the method further comprises the step of saving the document, including the embedded plurality of predefined elements, for use by internal/external engineers as formatted preparatory to creating the database. Also claim 4 has been amended to recite that the method further comprises using the saved document as formatted and saving the used document to a text-only document which can be utilized by the document reader script. Claims 11 & 12 have been amended to provide corresponding system

claims. The Applicant notes that Roesner does not disclose or suggest the features of the amended claims 3-5 and 11-13.

The Applicant therefore submits that the rejection to claims 1-15, 18 and 19 has been traversed. Applicant respectfully requests withdrawal of these rejections.

III.   Claim Rejections Under 35 U.S.C. §103

Requirements for Prima Facie Obviousness

The obligation of the Examiner to go forward and produce reasoning and evidence in support of obviousness under 35 U.S.C. §103 is clearly defined at M.P.E.P. §2142:

> The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness.

M.P.E.P. §2143 sets out the three basic criteria that a patent examiner must satisfy to establish a *prima facie* case of obviousness necessary for establishing a rejection to a claim under 35 U.S.C. §103:

1. some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings;

2. a reasonable expectation of success; and

3. the teaching or suggestion of all the claim limitations by the prior art reference (or references when combined).

It follows that in the absence of such a *prima facie* showing of obviousness under 35 U.S.C. §103 by the examiner (assuming there are no objections or other

grounds for rejection), an Applicant is entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443 (Fed. Cir. 1992).

Thus, in order to support an obviousness rejection under 35 U.S.C. §103, the Examiner is obliged to produce evidence compelling a conclusion that each of the three aforementioned basic criteria has been met.

Roesner in view of Aleksic

Claims 16-17 and 20 were rejected by the Examiner under 35 U.S.C. §103(a) as being unpatentable over Roesner et al, hereinafter "Roesner" (U.S. PG Pub 2004/0216077), in view of Aleksic et al (US 5,995,736), hereinafter Aleksic.

The Examiner argued that Roesner discloses all the limitations as set forth above in relation to the rejection to the claims under 35 U.S.C. §102(e).

The Examiner asserts that Aleksic discloses an automatic register generator (--RTL auto-generation module--) (Aleksic, fig. 3, element 36, which is associated with VDHL Design file (element 62))(col.5 II.36-67) for generating define statements utilized by an RTL code to decode and configure at least one hardware memory and at least one register (--memory model and register block--) thereof (col.5, II36-67 and fig. 6, col. 9 II. 20-29). The Examiner also asserts that Aleksic also discloses a software auto-generation module (--software device model --) that auto-generates a same set of define statements utilized by a software code thereof (fig. 3 and fig. 6 col. 9-12).

The Examiner argues that "it would have been obvious to one of ordinary skill in the art to combine Roesner and Aleksic references implementing a system work in two modes in order to satisfy the design development cycle and providing simultaneous generating of the behaviors model code and the hardware design simulation code from a single specification file have both outputs are consistent that provides more freedom and flexibility during the programming model phase of the design for experimentation in register layout".

The Applicants respectfully disagree with this assessment. The Applicant submits that it would not have been obvious to one of ordinary skill in the art to combine Roesner and Aleksic. Roesner is directed to a method and system for specifying and using a dial having a default value to configure a digital system. Aleksic is not directed to using a dial and, contrary to the Examiner's assertion, there is nothing in Aleksic to encourage the person of ordinary skill to modify Roesner to provide the subject-matter of old claims 16-17 and 20.

In any event, claims 16-17 and 20 are dependent on claims 8 & 18 as now amended which are limited to the plurality of predefined elements being embedded within the hardware specification document preparatory to storing the plurality of predefined elements in the database, such that said plurality of predefined elements comprise flags which can be utilized by a document reader script.

Aleksic discloses register data representing group data which is arranged in a format to be populated into register templates (see FIG.5, elements 82-88 and column 7, lines 18-40). Aleksic does not disclose or suggest embedding a plurality of predefined elements in a hardware specification document nor that the predefined elements comprise flags which can be utilized by a document reader script. As already mentioned above in relation to claim 1, embedding the predefined elements in the specification document using flags preparatory to storing the predefined elements in the database permits the user to more easily view and modify operational information in the specification document during the design or development of the circuit and still change the document into RTL code for the purpose of testing the functionality of the circuit.

There is nothing disclosed in Aleksic to encourage the person of ordinary skill to modify Roesner to obtain all the features of amended claims 1, 8 and 18.

Thus, with regard to amended independent claims 1, 8 & 18 and the claims dependent therefrom, at least the first and third prongs of the aforementioned test that must be satisfied to establish a *prima facie* case of obviousness necessary for establishing a rejection to a claim under 35 U.S.C. §103 are not met. There is no suggestion or motivation, either in Roesner or Aleksic themselves or in the knowledge generally available to one of ordinary skill in the art, to modify Roesner or to combine the teachings of Roesner and Aleksic so as to provide the claims' limitations and there is no teaching or suggestion of all the claims' limitations by Roesner and Clark taken alone or in combination.
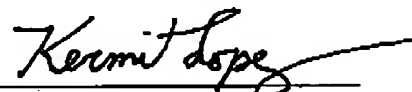
Therefore, since claims 16-17 and 20 are dependent on amended claims 8 and 18, the Applicants submit that the rejection to claims 16-17 and 20 have been traversed and should be withdrawn. The Applicants therefore respectfully request that the rejection to claims 16-17 and 20 be withdrawn.

III. Conclusion

In view of the foregoing discussion, the Applicants have responded to each and every rejection of the Official Action. The Applicants have clarified the structural distinctions of the present invention by discussions herein. The foregoing discussion and amendments do not present new issues for consideration and no new search is necessitated. Such amendments are supported by the specification and do not constitute new matter. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejections and further examination of the present application.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the undersigned representative to conduct an interview in an effort to expedite prosecution in connection with the present application.

Respectfully submitted,

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